THE INVENTION CLAIMED IS:

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1. An integrated circuit chip comprising:

a semiconductor substrate;

a semiconductor device over said semiconductor substrate;

a dielectric layer formed over said semiconductor substrate and said semiconductor device, said dielectric layer having a channel opening and a via provided therein; said via having a via entrant angle formed with said channel opening of greater than about 69 degrees whereby said channel opening forms a collimator for said via;

a seed layer lining said channel opening and said via; and

a conductive layer damascened into said seed layer and said dielectric layer whereby said conductive layer in said channel opening is operatively connected by said conductive layer in said via to said semiconductor device without voids.

2. The integrated circuit chip as claimed in claim 1 including:

an adhesion/barrier layer disposed between said dielectric layer and said seed layer in said channel opening and said via, said via with said adhesion/barrier layer having an adhesion/barrier layer via entrant angle formed with an adhesion/barrier layer channel opening of greater than about 70 degrees whereby said adhesion/barrier channel opening forms a collimator for said adhesion/barrier layer via.

3. The integrated circuit chip as claimed in claim 2 including:

said adhesion/barrier layer deposited by a process selected from a group comprising physical vapor deposition, chemical vapor deposition, and a combination thereof.

4. The integrated circuit chip as claimed in claim 3 wherein:

said adhesion/barrier layer of a material selected from a group comprising titanium, tantalum, tungsten, titanium nitride, tantalum nitride, tungsten nitride, and a combination thereof.

5. The integrated circuit chip as claimed in claim 1 wherein:

said seed layer is formed by ionized metal plasma deposition.

6. The integrated circuit chip as claimed in claim 5 wherein:

said seed layer is formed of a material selected from a group comprising aluminum, copper, gold, silver, an alloy thereof, and a combination thereof.

7. The integrated circuit chip as claimed in claim 6 wherein:

said conductive layer is deposited by a process of electroplating.

8. The integrated circuit chip as claimed in claim 1 wherein:

said conductive layer is formed of a material selected from a group comprising aluminum, doped polysilicon, copper, gold, silver, an alloy thereof, and a combination thereof.

9. The integrated circuit chip as claimed in claim 1 wherein:

said via has a high-aspect ratio.

10. The integrated circuit chip as claimed in claim 1 wherein:

said seed layer is of a relatively uniform thickness in said channel opening and said via.

11. An integrated circuit chip comprising:

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a semiconductor substrate;

a semiconductor device on said semiconductor substrate;

a first channel dielectric layer formed over said semiconductor substrate and said semiconductor device, said first channel dielectric layer having a first channel opening provided therein;

a first seed layer lining said first channel opening in said first channel dielectric layer;

a first conductive layer damascened into said first seed layer and said first channel dielectric layer whereby said conductive layer in said first channel opening is operatively connected to said semiconductor device;

second channel and via dielectric layers formed over said first channel dielectric layer, said second channel and via dielectric layers having a second channel opening and a via provided therein; said via having a via entrant angle formed with said second channel opening of greater than about 69 degrees whereby said second channel opening forms a collimator for said via;

a second seed layer lining said second channel opening and said via; and

a second conductive layer damascened into said second seed layer and said second channel dielectric and via layers whereby said second conductive layer in said

Sub B2 > second channel opening is connected by said second conductive layer in said via to said first conductive layer in said first channel without voids.

12. The integrated circuit chip as claimed in claim 11 including:

a second adhesion/barrier layer disposed between said second channel dielectric layer and said second seed layer in said second channel opening and said via, said via with said adhesion/barrier layer having an adhesion/barrier layer via entrant angle formed with an adhesion/barrier layer channel opening of greater than about 70 degrees whereby said adhesion/barrier channel opening forms a collimator for said adhesion/barrier layer via.

13. The integrated circuit chip as claimed in claim 12 including:

said second adhesion/barrier layer deposited by a process selected from a group comprising physical vapor deposition, chemical vapor deposition, and a combination thereof.

14. The integrated circuit chip as claimed in claim 13 wherein:

said second adhesion/barrier layer of a material selected from a group comprising titanium, tantalum, tungsten, titanium nitride, tantalum nitride, tungsten nitride, and a combination thereof.

15. The integrated circuit chip as claimed in claim 11 wherein:

said second seed layer is formed by ionized metal plasma deposition.

16. The integrated circuit chip as claimed in claim 15 wherein:

said second seed layer is formed of a material selected from a group comprising aluminum, copper, gold, silver, an alloy thereof, and a combination thereof.

17. The integrated circuit chip as claimed in claim 16 wherein:

said second conductive layer is deposited by a process of electroplating on said second seed layer.

18. The integrated circuit chip as claimed in claim 11 wherein:

said second conductive layer is formed of a material selected from a group comprising aluminum, doped polysilicon, copper, gold, silver, an alloy thereof, and a combination thereof.

19. The integrated circuit chip as claimed in claim 11 wherein:

said via has a high-aspect ratio of diameter to depth in excess of 1:2.

20. The integrated circuit chip as claimed in claim 11 wherein:

said second seed layer is of a relatively uniform thickness in said second channel opening and in said via.